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Design and Analysis of Power and Area Efficient 2/3 Prescaler Using E-TSPC Logic

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Abstract- One of the important functional blocks in frequency synthesizers is the high speed dual modulus prescaler. The bottleneck of the dual modulus prescaler design is that it operates at the highest frequencies and consumes more power than any other circuit blocks of the synthesizer. A dual modulus prescaler (also known as divide-by-N/N+1 counter) usually consists of a divide-by-2/3 prescaler unit followed by several asynchronous divide-by-2 units. In general, a divide-by-N/N+1 counter consist of flip flops and some extra logic implemented using logic gates which determine the terminal count. Here an E-TSPC logic based divide-by-2/3 prescaler suitable for low supply voltage (0.9V) and low power applications is been designed and implemented wherein the counting logic and the mode selection control are implemented using a single transistor. Thus the critical path is reduced which in turn enhances its working frequency. Simulation results show that, compared with the conventional TSPC and E-TSPC based 2/3 prescaler designs as much as 46% in PDP, 24% in operation speed and 44% in area can be achieved by the proposed design. Also a 32/33 prescaler, 47/48 prescaler and a multimodulus 32/33/47/48 prescaler which incorporates the proposed 2/3 prescaler are designed and implemented. Simulation results show that the power dissipation of the proposed multimodulus prescaler is lesser than the existing multimodulus prescaler designs. All prescalers were designed using the same 0.18µm TSMC CMOS process technology and simulated using Mentor Graphics ELDO.

Index Terms-Extended True Single Phase flip flops (ETSPC FFs), prescaler, low power, and low voltage

1 INTRODUCTION

One of the critical functional blocks in frequency synthesizers is the high speed dual modulus prescaler. It operates at the highest frequencies and consumes more power than any other circuit blocks of the frequency synthesizer. Hence the design of dual modulus prescaler is so crucial. A dual modulus prescaler usually consists of a divide-by-2/3 prescaler unit followed by several asynchronous divide-by-2 units. For example the topology of a divide-by-8/9 prescaler is implemented in the work done by Xiao Peng Yu [1] which has one 2/3 prescaler unit and two divide-by-2 units. In general a divide-by-N/N+1 counter (otherwise named as prescaler) consists of flip flops and some extra logic implemented using logic gates which determines the terminal count. Various flip-flop based designs have been proposed to improve the operating speed of dual-modulus prescalers (also called divide-by-N/N+1 counter). Conventional flip flop based N/N+1 counter designs suffer from large load capacitance which limits the maximum operating frequency which in turn increases the power consumption. Therefore, dynamic and sequential circuit techniques [2-4] or clocked logic gates such as, True Single Phase Clocks (TSPC) have to be used to reduce the circuit complexity, power dissipation and increase the operation speed. TSPC logic based designs can be further enhanced by using the Extended True Single Phase Clock (E-TSPC) logic. E-TSPC logic based designs are more suitable for high speed and low power applications. In this logic it removes the transistor stacked structure and thus they are more sustainable for low VDD operations. So here in this paper an E-TSPC logic based divide-by-2/3 prescaler design suitable for low supply voltage and low power consumption applications is been proposed. Here the counting logic and the mode selection control are implemented using a single transistor. So this eventually reduces the critical path and hence the operating frequency also increases.

Here the objective is to design and implement an E-TSPC based 2/3 prescaler which uses only a single transistor to implement the counting logic as well as the mode selection control. The power dissipation, delay and area of the proposed prescaler should not be much greater than the conventional prescalers. Also design and implement a 32/33 prescaler, 47/48 prescaler and a multimodulus 32/33/47/48 prescaler incorporating the proposed 2/3 prescaler. The power dissipation and the delay of the proposed multimodulus prescalers should also not be much greater than the existing multimodulus prescaler.

An idea of different existing prescaler designs which include both TSPC and E-TSPC based designs is given in section 2. Next, the description of our proposed 2/3 prescaler, 32/33 prescaler, 47/48 prescaler and multimodulus 32/33/47/48 prescaler is given in section 3. The comparative results based on our proposed approach

using Mentor Graphics ELDO Spice are given in section 4.

2 CONVENTIONAL DESIGNS

Dual-modulus or multi modulus division gives the flexibility to select channels on the basis of the number of times each of the moduli is selected.

2.1 DESIGN I- 2/3 PRESCALER BY PELLERANO

A divide-by-2/3 counter design based on E-TSPC logic proposed by Pellerano [7] is given in Figure 1. This design consists of two E-TSPC based flip flops (FFs) and two logic gates i.e., an OR gate and an AND gate. The transistor schematic of the design is depicted in the Figure 2. When the divide control signal DC is "0", the OR gate becomes disabled. The OR gate is merged into the output of FF1 as shown in the transistor schematic. The state of (Q1b, Q2b) cycles through 11, 01, and 00 states repetitively; this corresponds to a divide-by-3 function. When the divide control signal DC s "1", the OR gate has got a steady high output irrespective of the other input. So the output of FF1 will be disabled. Therefore FF2 alone performs the divide-by-2 function. But the major disadvantage with this approach is that there exists redundant power consumption during divide-by-2 operation due to the continuous toggling of FF1 output since the input to the FF1 is not disabled.

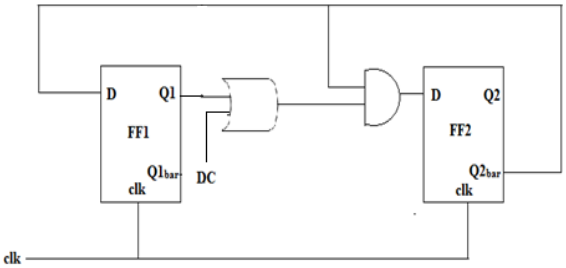

Figure 1: Logic Structure of Design I

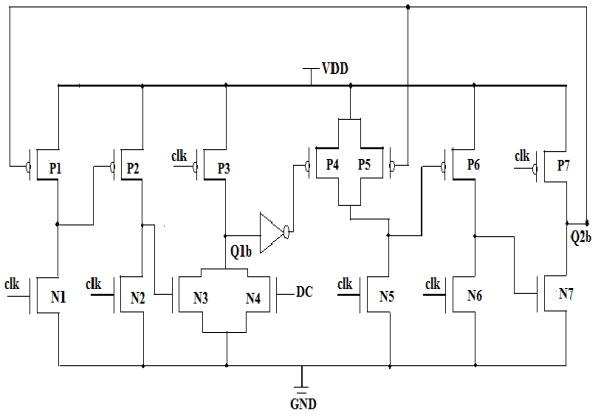

Figure 2: Transistor schematic of Design I

2.2 DESIGN II-2/3 PRESCALER BY PENG YU

As a remedy to the above mentioned problem in Design I, another divide-by-2/3 counter design based again on E-TSPC logic was proposed in [1] by Xiao Peng Yu as shown in Figure 3. Here the divide control logic is placed at the input of FF1 rather than at the output of FF1 as in Design I. The transistor schematic of the design is also depicted in the Figure 4. When DC_{bar}="0", output of FF1 becomes frozen i.e.; the output of AND gate is always 0 which makes the input to FF1 always steady. This prevents the following stages from any switching or toggling activities for the purpose of power saving and thus FF2 alone performs divide-by-2 function. But the cone here when compared to Design I is that the first stage of FF1 itself, however, encounters larger power consumption since the pull up path is turned on all the time and the short circuit current is drawn repetitively whenever the clock signal turns "1". An improved speed and low power 2/3 prescaler implemented in the TSPC logic style, Design III, is proposed by Vamshi Krishna [9] similar to the prescaler in [8], the proposed prescaler uses two embedded NOR gates instead of an AND gate and an OR gate as the conventional TSPC 2/3 prescaler. A wide-band multi-modulus 32/33/47/48 prescaler, Design IV, which can divide the input frequency by 32, 33, 47 and 48 respectively proposed by Vamshi [9], is depicted

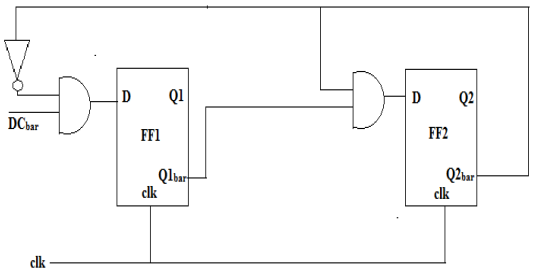

Figure 3: Logic Structure of Design II

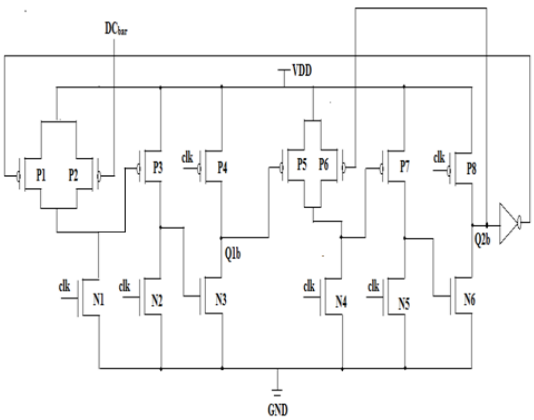

Figure 4: Transistor schematic of Design II

3 PROPOSED E-TSPC BASED 2/3 PRESCALER

An extended true-single-phase-clock (E-TSPC) based divide-by-2/3 counter design for low power consumption applications is proposed here. The logic structure of the proposed design is shown in Figure 5. As in previous E-TSPC based designs, Design I and Design II, the proposed design also has two flip flops (FFs) and an AND gate in common. The division control logic is implemented by means of a switch.

3.1 WORKING PRINCIPLE

As already stated above the division control logic is implemented here using a switch. When the switch is open, the input from FF1 is disconnected and FF2 alone comes into action and divides the clock frequency by 2. When the switch is close, similar to the Design I and Design II [1, 7], FF1 and FF2 are linked to form a counter with three distinct states and thus divides the clock frequency by 3. Figure 11 shows the circuit schematic of the proposed design. Other than the two E-TSPC FFs, only one PMOS transistor P_{DC} is needed. The PMOS transistor controlled by the divide control signal serves as the switch. The AND gate plus its input inverter are achieved by way of wired-AND logic using no extra transistors at all.

When DC is "1", the PMOS transistor P_{DC} is turned off as a switch should behave. A single PMOS transistor, however, presents a smaller capacitive load to FF1 than an inverter does in Design I [7]. When DC is "0", the output of FF1, Q1b, is connected with the output node of the first stage inverter of FF2 (D2b) through the PMOS transistor P_{DC}. In an E-TSPC FF design, the output of the first stage inverter can be regarded complementary to the input, D i.e., D_{bar}. Therefore, a wired-OR logic is actually implemented.

$$D2b=Q1b+Q2b_{bar}$$

By applying DeMorgan's law to the above Boolean equation we get,

$$D2b_{bar}=D2=Q1b_{bar}.Q2b$$

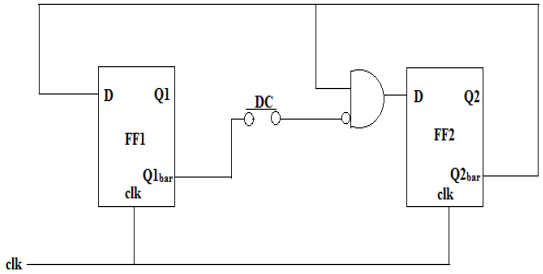

Figure 5: Logic Structure of the Proposed Design

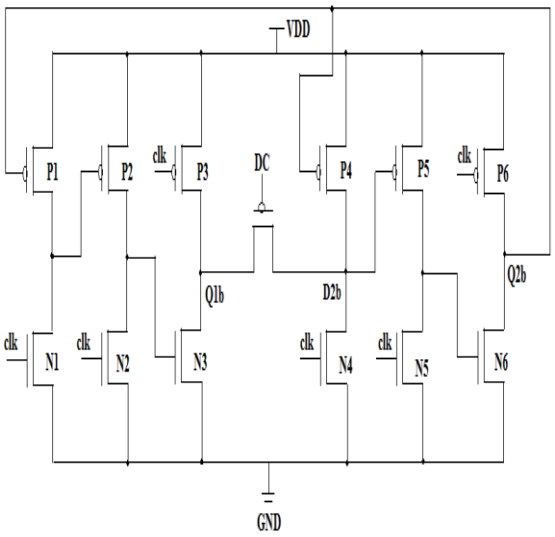

Figure 6: MOS Schematic of the Proposed Design

which is exactly the desired logic as it is quite evident from Figure 10. Since Q1b is applied to the input of D2b (complement of D), the inverter needed to complement the Q1b signal can be eliminated which makes the circuit more simple enhancing the speed and power behaviors.

First of all, unlike any previous designs, here the E-TSPC FF design remains intact without any logic embedding thereby the effect of parasitic capacitance is alleviated. Both speed and power behaviors are not affected, which indicates a performance edge over the logic embedded FF design. Secondly, the inverter to complement the one of the two E-TSPC FF outputs for divide-by-3 operations is removed in the proposed design. The circuit simplification, again, suggests the improvement in both speed and power performances.

Table 1 shows the state transition table and the excitation logic of Q1b, Q2b when working in the divide-by-3 mode.

Current State	Input Signal			Next State
(Q1b, Q2b)	D1=Q2b	$D2=Q1b_{bar}.Q2b$	$D2b=Q1b+Q2b_{bar}$	(Q1b_n, Q2b_n)
11	1	0	1=1+0	01
01	1	1	0=0+0	00
00	0	0	1=0+1	11
10	0	0	1=1+1	11

Table 1: State Transitions in divide-by-3 operation

3.2 PROPOSED 32/33 PRESCALER

A divide 32/33 dual modulus unit [10] incorporating the proposed 2/3 prescaler is implemented as shown in Figure 7. In this 32/33 prescaler, the 2/3 prescaler unit is followed by four stages of the toggled TSPC divide-by-2 units.

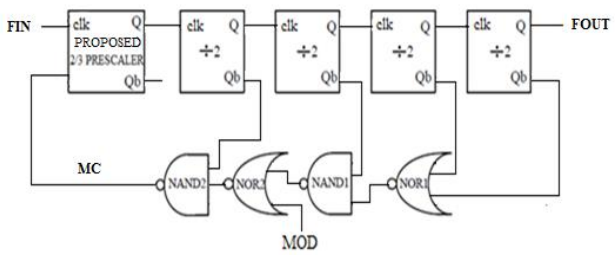

Figure 7: 32/33 prescaler using Proposed 2/3 prescaler

When the control signal MOD is '1', the output of NOR2 always remains at logic '0' and forces the output of NAND2 to logic '1' irrespective of data on Qb1. Since MC is always equal to logic '1', 2/3 prescaler remains in divide-by-2. Thus the 32/33 prescaler acts as divide-by-32 circuit. If we denote the synchronous 2/3 prescaler as M/M+1 and the four asynchronous dividers whose division ratio equal to 16 by 'AD', the division ratio in this mode (MOD='1') is given by

$$f_{32} = (AD - MOD_{bar}) * M + MOD_{bar} * (M+1) = (16-0) * 2 + 0 * (2+1) = 32$$

The dual-modulus 32/33 prescaler operates as divide-by-33 when MOD='0'. During this operation, the 2/3 prescaler operates in divide-by-2 mode for 30 input clock cycles and for the remaining 3 input clock cycles it operates in divide-by-3 mode. The division of the 32/33 prescaler in this mode is given by

$$f_{33} = (AD - MOD_{bar}) * M + MOD_{bar} * (M+1) = (16-1) * 2 + 1 * (2+1) = 33$$

3.3 PROPOSED 47/48 PRESCALER

A divide 47/48 dual modulus unit is implemented with the proposed 2/3 prescaler as shown in Figure 8. The proposed 47/48 prescaler circuit is similar to the 32/33 prescaler except for an additional inverter which is added between the output of the NAND2 gate and the control signal (MC) input of the 2/3 prescaler. The 47/48 prescaler consists of a 2/3 prescaler, four asynchronous divide-by-2 circuits and additional logic gates to control the division ratio between 47 and 48. Similar to the division ratios of 32 and 33, the division ratios of 47 and 48 are given below.

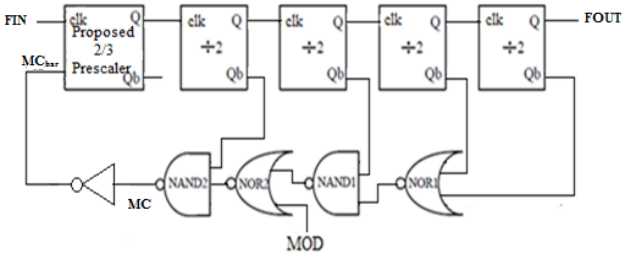

Figure 8: 47/48 prescaler using Proposed 2/3 prescaler

$$f_{48} = (AD - MOD_{bar}) * (M+1) + MOD_{bar} * M = (16-0) * (2+1) + 0 * 2 = 48$$

$$f_{47} = (AD - MOD_{bar}) * (M+1) + MOD_{bar} * M = (16-1) * (2+1) + 1 * 2 = 47$$

3.4 PROPOSED MULTIMODULUS 32/33/47/48 PRESCALER

The proposed wide-band multi-modulus 32/33/47/48 prescaler which can divide the input frequency by 32, 33, 47 and 48 respectively is shown in Figure 9. The multi-modulus prescaler is similar to the 32/33 and 47/48 prescaler but with an additional multiplexer to control the switching between 32/33 and 47/48 modes. The proposed prescaler performs additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and design complexity. Besides the usual MOD signal for controlling the division ratios (N/N+1), the additional control signal Sel is used to switch the prescaler between 32/33 and 47/48 modes.

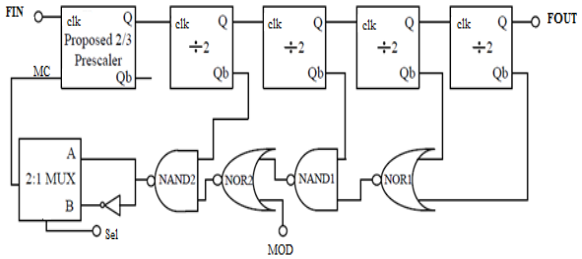

Figure 9: Proposed Multi modulus 32/33/47/48 Prescaler

4 SIMULATION RESULTS

All prescalers were designed using 0.18µm Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC) process technology. The schematic entry was done using Mentor Graphics Design Architect. The post layout Simulation was done using Mentor Graphics ELDO. Delay and energy were averaged over a set of random input vectors and the layout was done using Mentor Graphics IC Station.

4.1 2/3 PRESCALER SIMULATION

All the 2/3 prescaler designs such as Design I, Design II, Design III and the proposed prescaler were simulated. Since voltage scaling serves as the principal means for energy reduction, all simulations were conducted with a supply voltage of 0.9V for E-TSPC based circuits and 1.2V for TSPC based circuits as E-TSPC based circuits are sustainable to low VDD operations. The simulation results were analyzed and the total power dissipated was recorded in each case. The Pre layout simulation result of the proposed design is given in Figure 10 (a) and 10 (b).

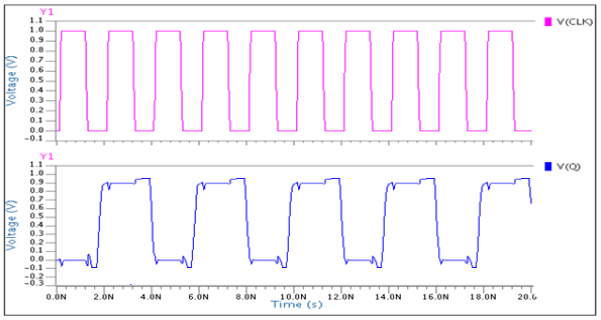

Figure 10 (a): Divide by 2 of Proposed Design

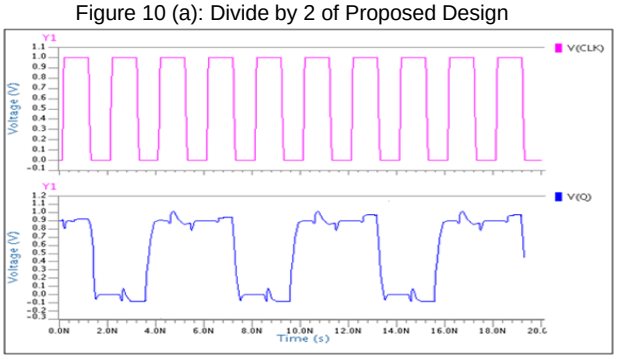

Figure 10 (b): Divide by 3 of Proposed Design

4.2 POWER, DELAY AND AREA COMPARISON

The power dissipation of all the 2/3 prescalers implemented is shown on table 2. The comparison results show that the proposed 2/3 prescaler has improved power performance than other designs. The comparison results show that the Power Delay Product (PDP) is less in the proposed design when compared to other implementations. The area was compared after taking layout of all the designs and the layout diagram of the proposed design was obtained. Therefore the proposed design has got 46%, 43% and 39% improved PDP when compared with Design I, Design II and Design III respectively. Also the speed performance is improved by 17%, 20% and 24% respectively.

Parameter	Design I	Design II	Design III	Proposed Design
Power Dissipated (µW)	14.23/19.74	12.98/17.06	11.47/17.73	9.152/12.96
PDP (fJ)	14.94/20.73	14.28/18.77	13.19/20.39	8.008/11.34
Area (µm^2)	129.60	132.48	211.50	118.50
# of Transistor Count	16	16	22	13

Table 2: Feature Comparison of 2/3 Prescalers

4.3 32/33 PRESCALER SIMULATION

The Pre–Layout simulation of the 32/33 prescaler design using the proposed prescaler was done. The simulation results were analyzed and the total power dissipated was recorded. The total power dissipated obtained are 20.8µW and 29.45µW in division by 32 and 33 modes respectively. The Pre-layout simulation results of the design are given below in Figure 11.

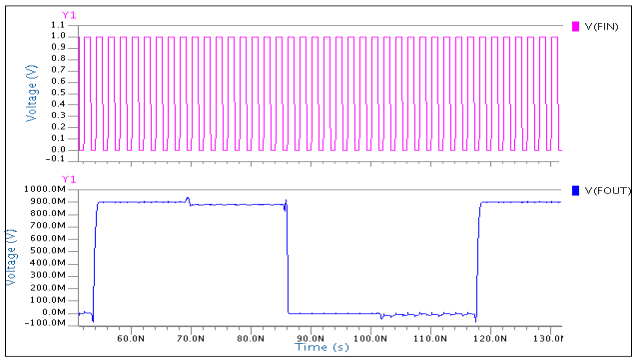

Figure 11 (a) Divide by 32 of 32/33 Prescaler

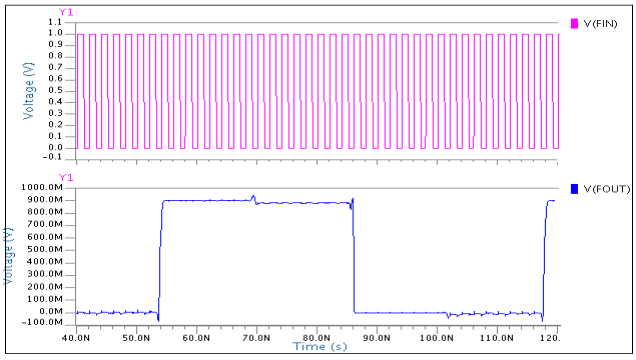

Figure 11 (b) Divide by 33 of 32/33 Prescaler

A. 4.4 47/48 PRESCALER SIMULATION

The Pre–Layout simulation of the 47/48 prescaler design using the proposed prescaler was done. The simulation results were analyzed and the total power dissipated was recorded. The total power dissipated obtained are 21.28µW and 30.13µW in division by 47 and 48 modes respectively. The Pre-layout simulation results of the design are given below in Figure 12.

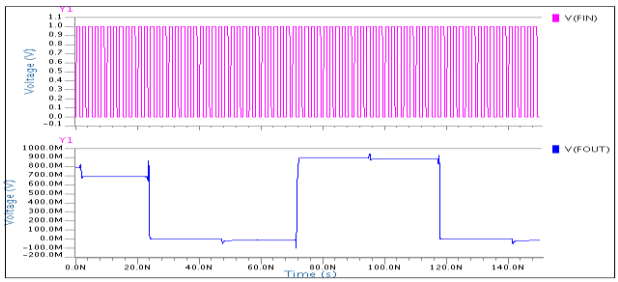

Figure 12 (a) Divide by 47 of 47/48 Prescaler

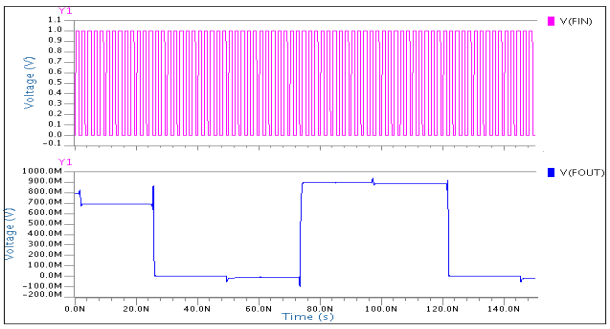

Figure 12 (b) Divide by 48 of 47/48 Prescaler

4.5 MULTIMODULUS 32/33/47/48 PRESCALER SIMULATION

The Pre–Layout simulation of the multimodulus prescaler design using the proposed prescaler was done. The simulation results were analyzed and the total power dissipated was recorded in each case. On comparison, it proves that the proposed multimodulus prescaler has 20% and 28% better power performance in N and N+ 1 division respectively. The simulation results are the same as shown in Figure 11 and Figure 12.

Multimodulus Prescaler Design	Power Dissipated (µW)	
	32/33	47/48
Design IV	26.36/41.29	26.97/42.08
Proposed Design	21.1/29.75	21.58/30.43

Table 3: Power and Delay Comparison of Multimodulus Prescalers

5 CONCLUSION

In the proposed design a 2/3 prescaler was implemented using E-TSPC logic. The proposed design is much more area efficient compared to the existing implementations due to the reduced number of transistors required for its implementation. Simulation results show that, compared with the conventional TSPC and E-TSPC based 2/3 prescaler designs as much as 46% in Power Delay Product (PDP), 24% in operation speed and 44% in area can be achieved by the proposed design. Also a 32/33 prescaler, 47/48 prescaler and a multimodulus 32/33/47/48 prescaler which incorporates the proposed 2/3 prescaler were designed and implemented. Simulation results show that the power dissipation of the proposed multimodulus prescaler is lesser than the existing multimodulus prescaler design. The schematic entry was done using Mentor Graphics Design Architect and simulation was done using Mentor Graphics ELDO. The simulation was done using TSMC 180nm process technology.

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